

Top Level Floorplan

FIG. 2

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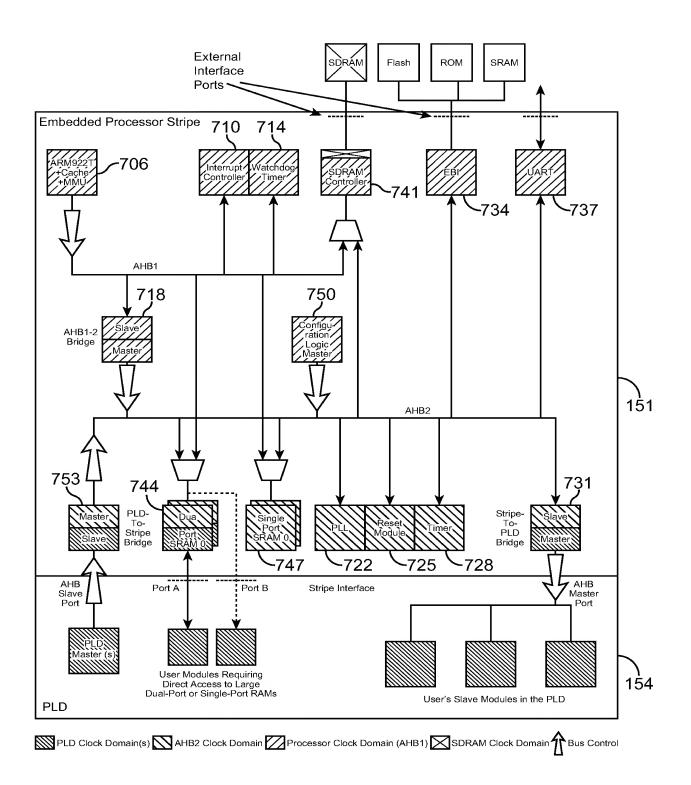


FIG. 7

+

PROGRAMMABLE LOGIC

FIG. 8

EMBEDDED PROCESSOR STRIPE

FIG. 9

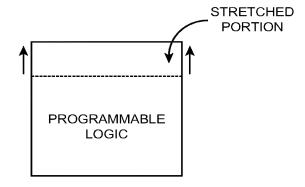


FIG. 10

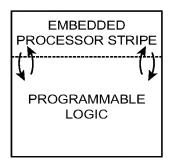
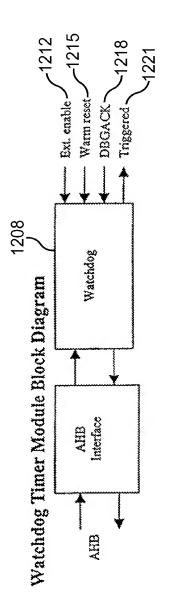


FIG. 11

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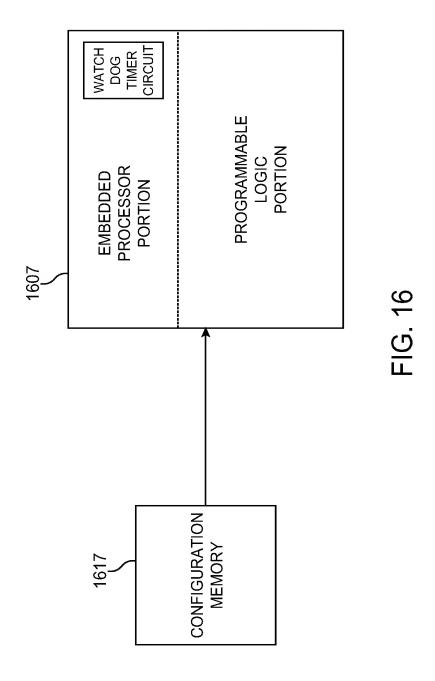


Access: Read/Write Address: Address Base + 0x4C0 Control Register (WDOG\_CR) - Read/Write Register: WDOG\_CR

0

0 means watchdog disabled. Other values specify bits 29:4 of the trigger value When this bit has the value I further writes to the register have no effect. Reserved for future use. Write as 0 to ensure future compatibility, (bits 3:0 of the trigger are always zero. cz. TRIGGER L.K. 0

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